

REMARKS

Claims 1-18 are pending in the present application. Claims 3, 6, and 18 stand rejected and claim 16 was objected to. The Examiner's reconsideration of the rejection is respectfully requested in view of the above amendment and the following remarks.

Applicant gratefully acknowledges the Examiner's indication that claims 1, 2, 4, 5, 7-15, and 17 are allowed.

Claim 16 was objected to for informalities, namely, the term "Wsix" should be "WSix". Claim 16 has been amended as suggested.

Claims 3 and 6 were rejected under 35 USC 112, first paragraph. The Examiner stated, "the specification does not disclose the unit of measurement for the dimensions of the layers described in claims 3 and 6."

Claims 3 and 6 have been amended to insert "angstrom" as the unit of measurement. The Specification has also been amended to insert the angstrom as the unit of measure. Those ordinary skilled in the art of fabricating flash memories can readily appreciate that unit of measurement for thickness of dielectric layers or oxide layers in a flash memory is in the order of angstroms. Thus, the insertion of "angstrom" as unit of measurement should not be construed as new matter.

Claim 18 was rejected under 35 USC 103 as unpatentable over Takebuchi in view of Komori and further in view of Sheu. The Examiner stated that, "Takebuchi does not disclose the use of silicide with common source line or contact. However, the use of silicide for contact structure is well known in the art. Komori discloses discloses that using a silicide in a contact plug has the benefit of reducing resistance which leads to an

overall increase in operation speed for a semiconductor device. Furthermore, Sheu discloses faster memory devices are a known goal in the art. Therefore, in view of Komori and Sheu, it would be obvious to use silicide with the common source line or contact in the device of Takebuchi.”

The rejection is respectfully traversed.

Applicant respectfully submits that the piecemeal collection of selected teachings from multiple references, with the benefit of hindsight reading of the teaching of the present application, to arrive at the elements of the claimed invention is improper. Further, even if Komori and Sheu can be combined to Takabuchi, the combination still fails to teach “a silicide layer on the exposed second conductive layer and the common source line”, as claimed in claim 18. Accordingly, claim 18 is not rendered obvious over Takabuchi in view of Komori and Sheu.

Claims 19 and 20 are added to further define the semiconductor structure as claimed in claim 18.

For the foregoing reasons, it is believed that the present application including claims 1-20, is in condition for allowance. Early and favorable actions is respectfully urged.

Respectfully submitted,



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